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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,579	02/01/2008	Mihai Adrian Tiberiu Sanduleanu	NL04 0105 US1	8721

65913 7590 06/19/2008
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EXAMINER

ROJAS, DANIEL E

ART UNIT	PAPER NUMBER
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2816

NOTIFICATION DATE	DELIVERY MODE
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06/19/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No. 10/588,579	Applicant(s) SANDULEANU ET AL.	
	Examiner DANIEL ROJAS	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☒ Claim(s) 1, 10-17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 August 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>8/4/2006</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. A preliminary examination of this application reveals that it includes terminology which is so different from that which is generally accepted in the art to which this invention pertains that a proper search of the prior art cannot be made. For example: in page 4, lines 16-18 of the specification, D+ is defined as an inverting input, D- is defined as a non-inverting input, Q+ is defined as an inverting output, and Q- is defined as a non-inverting output when the conventional terminology in the art is that a + terminal signifies non-inverting and a - terminal signifies inverting. Hence, D+ should be defined as a non-inverting input, D- should be defined as an inverting input, Q+ should be defined as a non-inverting output, Q- should be defined as an inverting output, CK+ should be defined as a non-inverting clock, and CK- should be defined as an inverting clock throughout the entire specification.

Applicant is required to provide a clarification of these matters or correlation with art-accepted terminology so that a proper comparison with the prior art can be made. Applicant should be careful not to introduce any new matter into the disclosure (i.e., matter which is not supported by the disclosure as originally filed).

A shortened statutory period for reply to this action is set to expire ONE MONTH or THIRTY DAYS, whichever is longer, from the mailing date of this letter.

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the claimed elements do not correspond to the elements in the

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figures (i.e. D+ should be changed to D-, D- should be changed to D+, Q+ should be changed to Q-, Q- should be changed to Q+, CK+ should be changed to CK-, and CK- should be changed to CK+). Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

3. Claims 1 and 10 are objected to because of the following informalities: all instances where the term "if" is used should be changed to "when." Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 7 recites the limitation "the second resistor means" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota (US Patent No. 4,841,168), hereinafter referred to as Kubota. Please refer to the figure below:

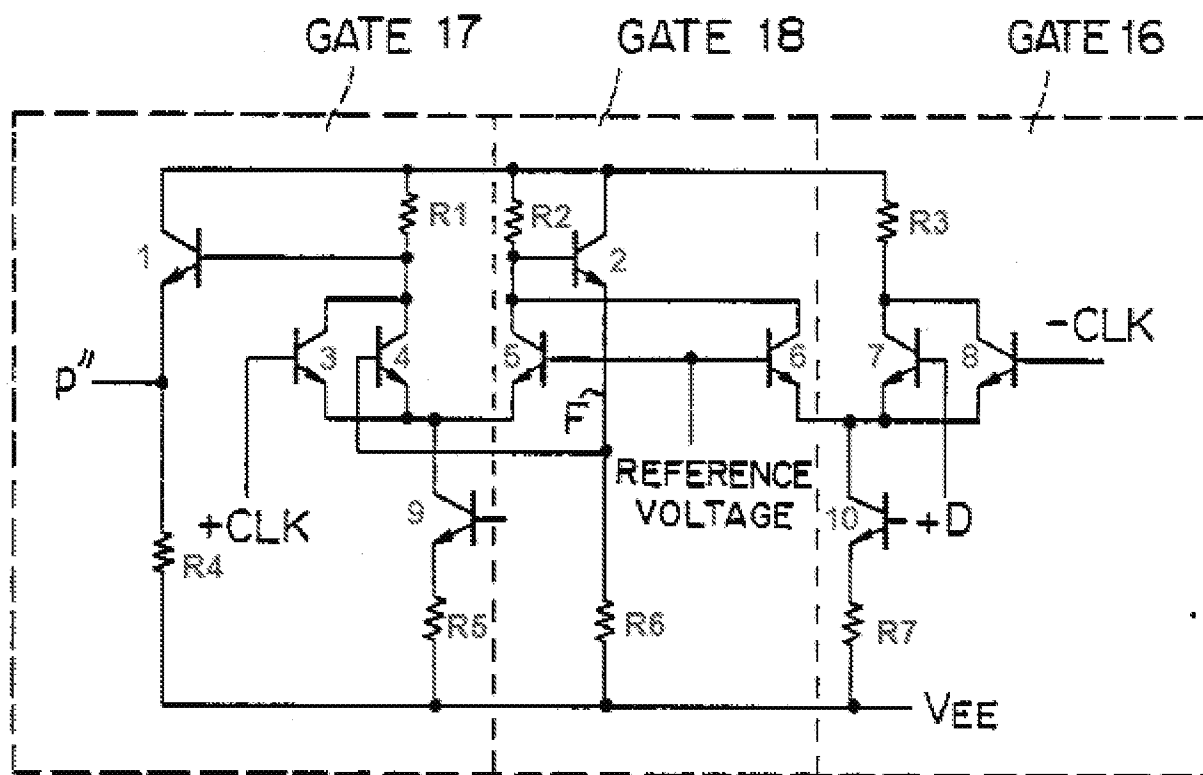


Figure 1: Kubota's gates 16, 17, and 18 at a transistor level

9. For claim 1, Kubota teaches in his Figure 5 (shown in detail in his Figure 8), a latch circuit comprising: a differential input with an inverting input (D input of 17) and a non-inverting input (input terminal of 16 connected to +D), one of the outputs (MASTER OUTPUT, which is a non-inverting output) being coupled to one of the inputs input (D-) having an opposite polarity, a control input for receiving a control signal (REFERENCE VOLTAGE, Figure 8) for determining a threshold for an input signal (D+, inherent in the structure of Figure 8) such that if the input signal is at larger than the threshold the non-inverting output in a HIGH logic state and in a LOW state if the input signal is smaller than the threshold (inherent based on the structure of Figure 8), respectively but fails to teach a differential output with an inverting output. However, examiner takes official notice that it is notoriously old and well known in the art to invert an output of a latch in order to change an active high output signal to an active low, for use with active low circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to branch off the MASTER OUTPUT signal into an inverter (i.e. a node from the MASTER OUTPUT signal being connected to the input of an inverter) in order to obtain an inverting output capable of use with active low circuits.

10. For claim 2, Kubota further teaches a latch circuit comprising transistors (as shown in Figure 8, with added numbering for reference in the figure above) the latch further comprising, a first pair of transistors comprising a first transistor (4) and a second transistor (5) having their sources coupled to each other (as shown), a second pair of transistors comprising a third transistor (6) and a fourth transistor (7) having their sources coupled to each other, a gate of the second transistor being coupled to a gate

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of the third transistor (as shown) and further coupled to the control signal (REFERENCE VOLTAGE), a positive feedback from the non-inverting output (F) to a gate of the first transistor (as also shown in Kubota's Figure 5), a pair of switches comprising a first switch (3) and a second switch (8) having their respective drains and sources coupled to the respective drains and sources of the first transistor and the fourth transistor, respectively, but fails to teach that the gate of the first switch being driven by the inverting clock signal (-CLK, as explained below) and gate of the second switch being driven by the non-inverting clock signal (+CLK, as explained below). The terms "inverted" and "non-inverted" are used to describe the state of a signal (i.e. inverted or not inverted) in relation to a second signal. Therefore, since both -CLK and +CLK are clock signals, +CLK can be considered an inversion of -CLK. Examiner takes official notice that it is notoriously old and well known to replace bipolar junction transistors with MOS transistors. Therefore, it would have been obvious to one of ordinary skill in the art to replace Kubota's bipolar junction transistors with MOS transistors in order to reduce space, since MOS transistors can be manufactured much smaller than bipolar junction transistors.

11. For claim 3, Kubota further teaches that the sources of the first transistor and the second transistor are supplied by a first current source (9), the sources of the third transistor and the fourth transistor are supplied by a second current source (10).

12. For claim 4, Kubota teaches the circuit of claim 3 but fails to teach that the first and second current source provide substantially equal currents. However, it would have been obvious to one of ordinary skill in the art to have the first and second current

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sources provide substantially equal currents since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F .2d 272, 205 USPQ 215 (CCPA 1980).

13. For claim 5, Kubota further teaches that the drain of the first transistor and the drain of the fourth transistor are coupled to each other and further coupled to a supply voltage (VEE) via a first resistor means (R6).

14. For claim 6, Kubota further teaches that the drain of the second transistor (5) is coupled to a drain of the third transistor (6), the drains being further coupled to the supply voltage (V_{EE}) via a second resistor means (R2).

15. For claim 8, Kubota teaches a first current source (9), a second current source (10) which receive a reference signal via their respective gates and a third resistor means (R5 and R7) but fails to teach a series connection of a main current channel of a current source. It is notoriously old and well known that if multiple nodes are receiving a reference signal of equal voltage, the said multiple nodes can be connected to a single reference voltage source. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have Kubota's first and second current source (9 and 10, respectively) connected to the same reference voltage source since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F .2d 272, 205 USPQ 215 (CCPA 1980).

16. For claim 9, it is inherent for a transistor to be controlled by a voltage applied to its gate. Therefore, the first and second current sources (9 and 10, respectively) are controlled by a voltage.

Allowable Subject Matter

17. Claims 10-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816